ABSTRACT

Error correction codes are a means of including redundancy in a stream of information bits to allow the detection and correction of symbol errors during transmission. The birth of error correction coding showed that Shannon's channel capacity could be achieved when transmitting information through a noisy channel. Turbo codes are a very powerful form of error correction codes that bring the performance of practical coding even closer to Shannon's theoretical specifications. Bit-error-rate (BER) performance and power dissipation are two important measures of performance used to characterize communication systems.

In digital communication systems, specifically wireless mobile communication applications, Size and Speed are dominant factors while meeting the performance requirements. According to the computational complexity of the employed decoding algorithms, such as Maximum A Posteriori probability (MAP), Bahl-Cocke-Jelinek-Raviv Algorithm (BCJR) and Soft Output Viterbi Algorithm (SOVA) the realization of turbo decoders usually takes a large amount of memory spaces and potentially long decoding delay. In Turbo decoders, MAP algorithm has been widely used for its optimum error correcting performance. But it is very difficult to design high-speed, Low Power and Memory Efficient MAP Decoder because of its

recursive computations. So, a sophisticated design of Max Log MAP (MLMAP) decoder is essential to obtain a better error correction in order to meet the current technological requirements.

Technique based on branch metric normalization is introduced to improve the speed performance of the decoder. Block Interleaved Pipelining (BIP) is a new high-throughput technique for ML MAP decoder is proposed in this work. An area-efficient symbol-based BIP MAP decoder architecture is also proposed by combining BIP with the well-known look-ahead computation in order to reduce the power consumption. The reverse calculation of state metrics is an efficient method to reduce memory accesses is also carried out in this work.

Efficient VLSI implementations are the key to enable high-performance, low power, High Speed, Memory efficient and low cost user equipments. The performance of Multiple Input Multiple Output (MIMO) technology critically depends on the employed data detection algorithm and corresponding high-performance methods usually entail very high complexity. In particular, a straightforward implementation of hard output Maximum Likelihood (ML) detection and soft-output A-Posteriori Probability (APP) detection provides excellent error rate performance. A dual binary MLMAP Decoder is proposed to share the hardware usage of the decoder and also greatly reduces the power consumption.

Therefore proper VLSI architecture is required to design a High Performance MAP decoder to meet out the requirements of current technology. This work proposes MAP decoding architecture with greater error correcting capability and lower computational hardware complexity. Decoding procedure of the conventional Max-Log-MAP algorithm are performed in parallel and formulated in to a set of simple operations, which can considerably increase the speed of the decoding operations and reduce the complexity of the algorithm.

In this research, a scalable MAP processor design is proposed which can support both single-binary (SB) and double-binary (DB) decoding for high throughput decoding. The memory requirement for storing the branch and state metrics can be reduced greatly, and synthesis result shows that the overall memory area can be reduced dramatically when compared to state-of-art MAP decoders. Decoder throughput of the proposed method is maintained without degrading the BER performance.